CMOSTEK

CMT2220LS

300 - 480 MHz OOK Receiver with 3.0 - 5.5 V Supply Power

Features

- Frequency range: 300 - 480 MHz
- Data rate: 1 - 5 kbps
- Sensitivity: -108 dBm (3 kbps), 0.1% BER
- Receiver bandwidth: 510 kHz @ 433.92 MHz
- Image rejection ratio: 33 dB
- Supporting input signal up to 10 dBm
- Operating independently with antenna in and data out
- Supply voltage: 3.0 – 5.5 V
- Low power consumption: 5.3 mA @ 315 MHz
- SOP8 packaging
- RoHS compliant

Application

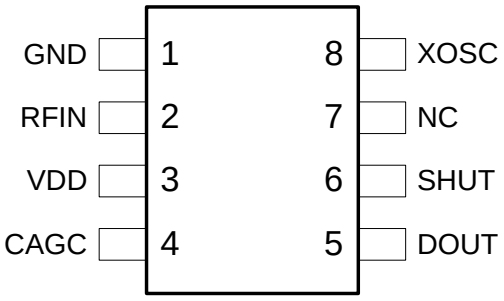
- Home and building automation control
- Infrared receiver replacement
- Industrial monitoring and control
- Wireless meter reading
- Wireless lighting control system
- Wireless alarm and security system
- Access control system with remote control

Description

The CMT2220LS are new-generation, low-power, high-performance, plug-and-play based OOK RF receiver with no need for register configuration, fitting for wireless receiving applications within 300 - 480 MHz ISM band. The CMT2220LS supports a data rate range of 1 - 5 kbps, ideal for pairing with encoder or MCU based low-cost transmitters. Operating in a supply voltage range of 3.0 - 5.5 V, the chip remains stable receiving performance with no significant performance change in different power supply voltage within this voltage range. It consumes only a current of 5.7 mA while achieving a receiving sensitivity of -108 dBm @ 433.92 MHz. The chip can operate at the commonly used 315 MHz frequency or other RF frequency points within the applicable frequency band through selecting crystals with different frequencies. The CMT2220LS receiver cooperating with CMT211x / 5x / 8x transmitters can fulfill cost-effective RF application solutions conveniently.

Ordering Information

Product Model	Package	Minimum Order Quantity
CMT2220LS-ESR	SOP8/Tape	2,500 pcs



CMT2220LS Pin Arrangement

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1 Electrical Specifications

If nothing else stated, the test conditions are V_{DD}= 5.0 V，T_{OP}= 25 °C，F_{RF} = 433.92 MHz, sensitivity being measured by receiving a PN9 sequence, matching to 50 Ω impedance and 0.1% BER. All measurement results are obtained using the evaluation board CMT2220LS-EM if nothing else stated.

1.1 Recommended Operating Conditions

Table 1. Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}	-40℃~ +85℃	3.0		5.5	V
Operating temperature	T_{OP}		-40		85	℃
RF supply voltage slope	V_{SL}		1			mV/us

1.2 Absolute Maximum Ratings

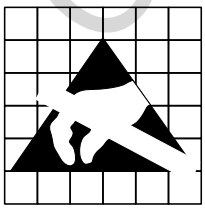
Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Condition	Min.	Typ.	Max.
Supply voltage	V_{DD}		-0.3	5.5	V
Interface voltage	V_{IN}		-0.3	V_{DD} + 0.3	V
Junction temperature	T_J		-40	125	℃
Storage temperature	T_{STG}		-50	150	℃
Soldering temperature	T_{SDR}	Lasts for at least 30 seconds		255	℃
ESD rating[2]		Human body model (HBM)	-2	2	kV
Latch-up current		@ 85 ℃	-100	100	mA

Notes:

[1]. Exceeding *the Absolute Maximum Ratings* may cause permanent damage to the equipment. This value is a pressure rating and does not imply that the function of the equipment is affected under this pressure condition, but if it is exposed to absolute maximum ratings for extended periods of time, it may affect equipment reliability.

[2]. The CMT2220LS is a high performance RF integrated circuit. The operation and assembly of this chip should only be performed on a workbench with good ESD protection.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent performance degradation or loss of functionality.

1.3 Receiver Specification

Table 3. Receiver Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F_{RF}	Through choosing crystals with different frequencies	300		480	MHz
Data rate	DR		1		5	kbps
Sensitivity	S_{315}	F_{RF} = 315 MHz, DR = 3 kbps, BER = 0.1%		-111		dBm
	$S_{433.92}$	F_{RF} = 433.92 MHz, DR = 3 kbps, BER =		-110		dBm
Operating current	I_{DD315}	F_{RF} = 315 MHz		5.3		mA
	$I_{DD433.92}$	F_{RF} = 433.92 MHz		5.7		mA
Shutdown current	I_{SHUT}	SHUT pin keeps high level		0.3		uA
Receiver bandwidth	BW_{315}	F_{RF} = 315 MHz		370		kHz
	$BW_{433.92}$	F_{RF} = 433.92 MHz		510		kHz
Receiver startup time [1]	$T_{START-UP}$	Time duration from the time point when SHUT pin changes from high level to low level to the time point when received data is output.		4		ms
Saturation input level	P_{LVL}			10		dBm
Input third-order Intercept point	IIP3	Two-tone test with frequency offset between 1 and 2 MHz, maximum system gain setting.		-29		dBm
Anti-blocking	BI	±1 MHz, continuous wave jamming		32		dB
		±2 MHz, continuous wave jamming		42		dB
		±10 MHz, continuous wave jamming		61		dB
Anti-co-channel-interference	CCR			-11		dB
Image rejection ratio	IRR			33		dB

Notes:

[1]. The receiver startup time is affected much by the CAGC capacitance value as well as the received signal strength. The less the signal strength, the longer the startup time.

- In AC to DC power supply systems, if an application allows a longer chip startup time, users can choose a CAGC with larger value. For instance, 4.7 uF is an appropriate value. In this case the chip startup time is around 70 ms in the condition of receiving signal strength being near to receiving sensitivity.
- In battery-powered applications, it is appropriate to select CAGC as 1 uF. In this case the chip startup time is around 8 ms in the condition of receiving signal strength being near to receiving sensitivity. If it requires a shorter chip startup time, users can choose a slightly smaller CAGC value based on practical requirements.

1.4 Crystal Oscillator Specification

Table 4. Crystal Oscillator Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency	$F_{XTAL315}$	F_{RF} = 315 MHz		9.81563		MHz
	$F_{XTAL433.92}$	F_{RF} = 433.92 MHz		13.52127		MHz
Crystal frequency tolerance [1]				±20		ppm
Load capacitance[2]	C_{LOAD}	49USSMD or 49S packaging		15		pF
Crystal equivalent resistance	Rm				60	Ω
Crystal startup time[3]	T_{XTAL}			400		us

Notes:

[1]. It involves:(1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature changing. The acceptable crystal frequency tolerance is subject to the bandwidth of the receiver and the RF tolerance between the receiver and its paired transmitter.

[2]. As the crystal parasitic capacitance value differs in different crystal packaging type, it is recommended to select a crystal with appropriate load capacitance value according to the packaging type used.

[3]. This parameter is to a large degree crystal dependent.

2 Pin Description

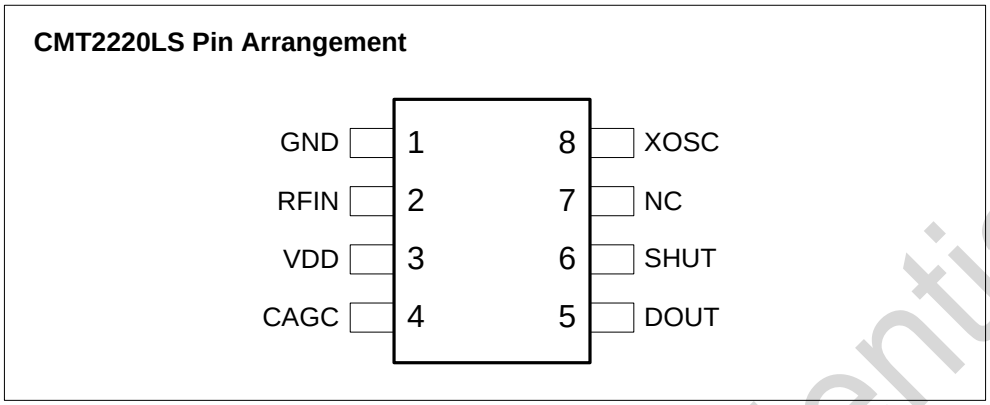


Figure 1. CMT2220LS Pin Arrangement Diagram

Table 5. CMT2220LS Pin Description

Pin #	Pin Name	I/O	Description
1	GND	I	Ground
2	RFIN	I	RF signal input pin, connecting matching network externally.
3	VDD	I	3.0 - 5.5 V supply power input.
4	CAGC	I	Automatic gain control pin, connecting filtering capacitor externally.
5	DOUT	O	Received data output
6	SHUT	I	Chip shutdown control pin, connecting high level to disable the chip and connecting low level to enable the chip.
7	NC	I	No connection
8	XOSC	I	Crystal oscillator input pin, connecting crystal externally.

3 Typical Application Schematic

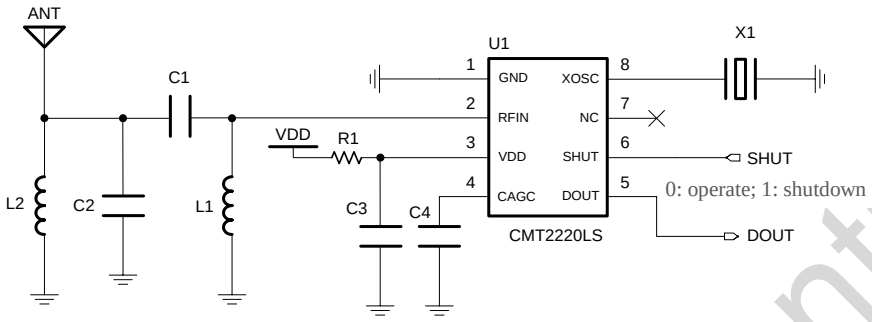


Figure 2. CMT2220LS Typical Application Schematic

Table 6. Typical Application BOM (Matching to 315 / 433.92 MHz)

Label	Description	Component Value		Unit	Supplier
		315 MHz	433.9 2MHz		
X1	Crystal, ±20 ppm, 49USSMD	9.81563	13.52127	MH	EPSON
L1	Matching network inductor, ± 10%, 0603 multilayer chip inductor	47	27	nH	Sunlord
L2	Matching network inductor, ± 10%, 0603 multilayer chip inductor	68	39	nH	Sunlord
C1	Matching network capacitor, ±0.25 pF, 0402 NP0, 50 V	4.7	2.7	pF	-
C2	Matching network capacitor, ±0.25 pF, 0402 NP0, 50 V	3		pF	-
C3	Supply power filtering capacitor, ±20%, 0603 X7R, 25 V	0.1		uF	-
C4[1]	Gain control filtering capacitor, ±20%, 0603 X7R, 25 V	4.7[1]	1[1]	uF	-
C5	Data filtering capacitor, ±20%, 0603 X7R, 25 V	0.47		uF	-
R1	Resistor, 5%, 1/8W, 0603	47		Ω	-
U1	CMT2220LS, 300 - 480 MHz OOK receiver with 3.0 - 5.5 V supply power	-		-	CMOSTEK

Notes:

[1]. The value of the gain control filtering capacitor will affect the receiver startup time much. Users can select an appropriate gain control filter capacitor (CAGC) according to the notes information specified in Table 3.

4 Typical Performance

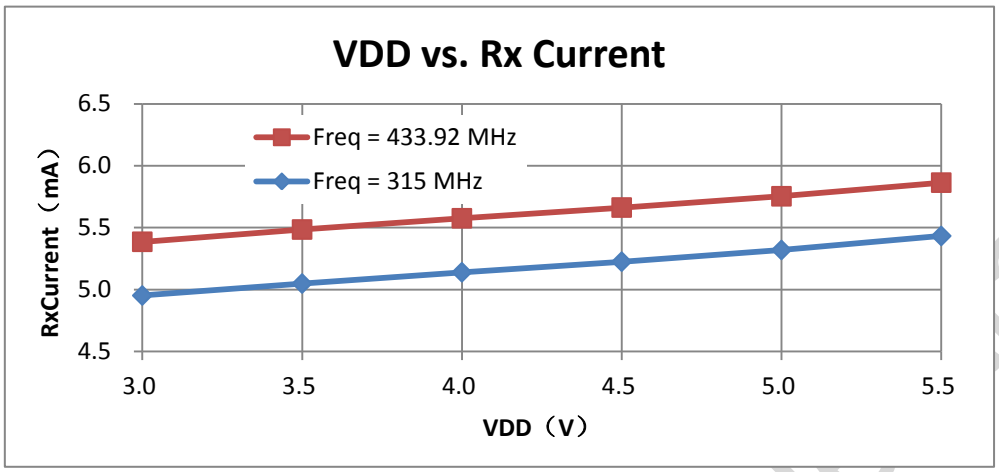


Figure 3. Rx Current vs. VDD

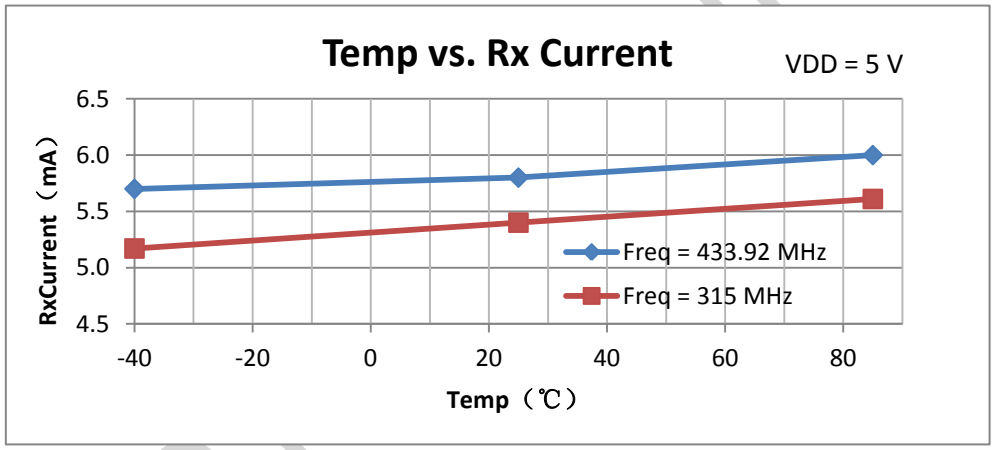


Figure 4. Rx Current vs. Operating Temperature

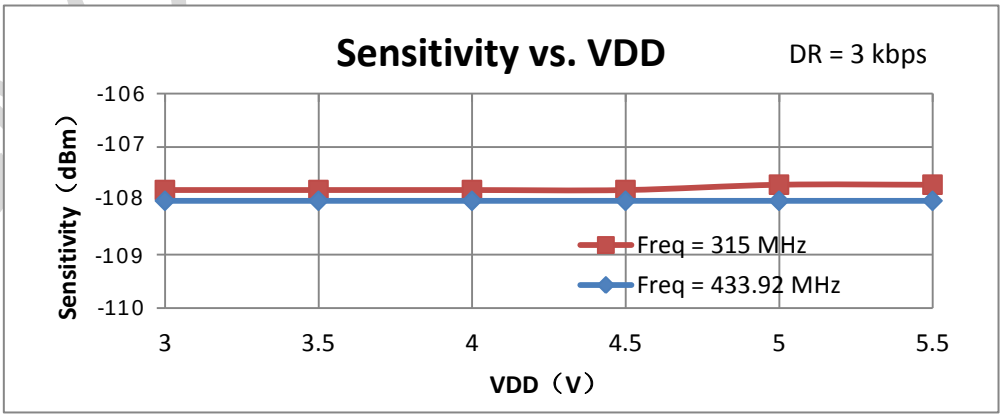


Figure 5. Sensitivity vs. VDD

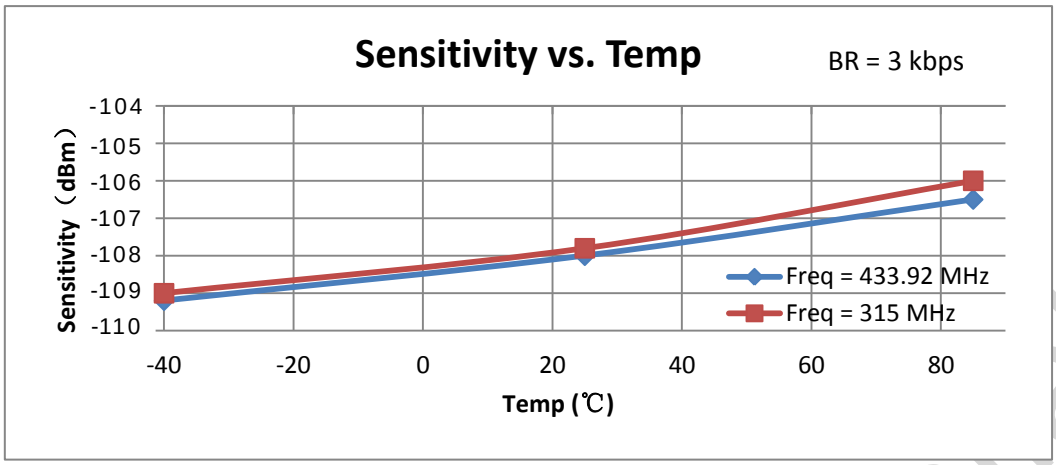


Figure 6. Sensitivity vs. Operating Temperature

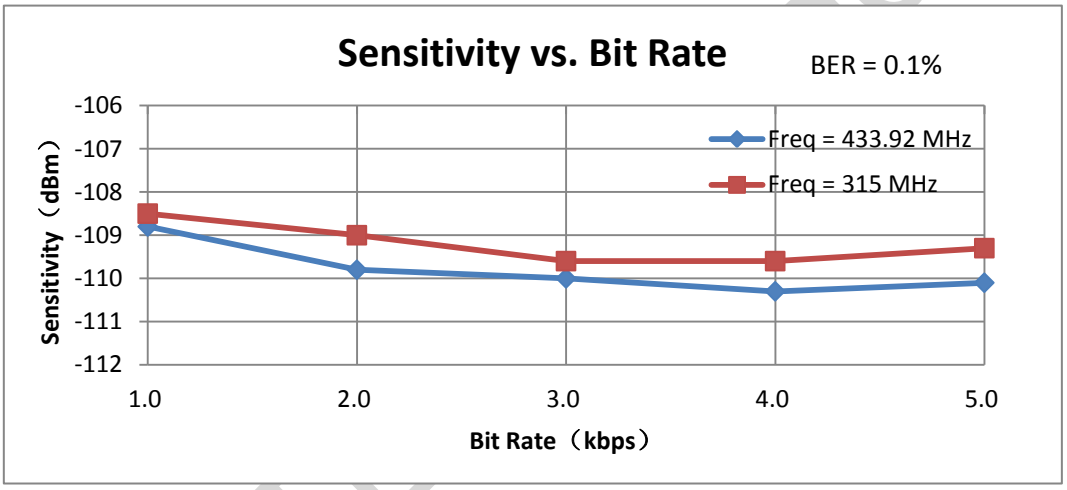


Figure 7. Sensitivity vs. Bit Rate

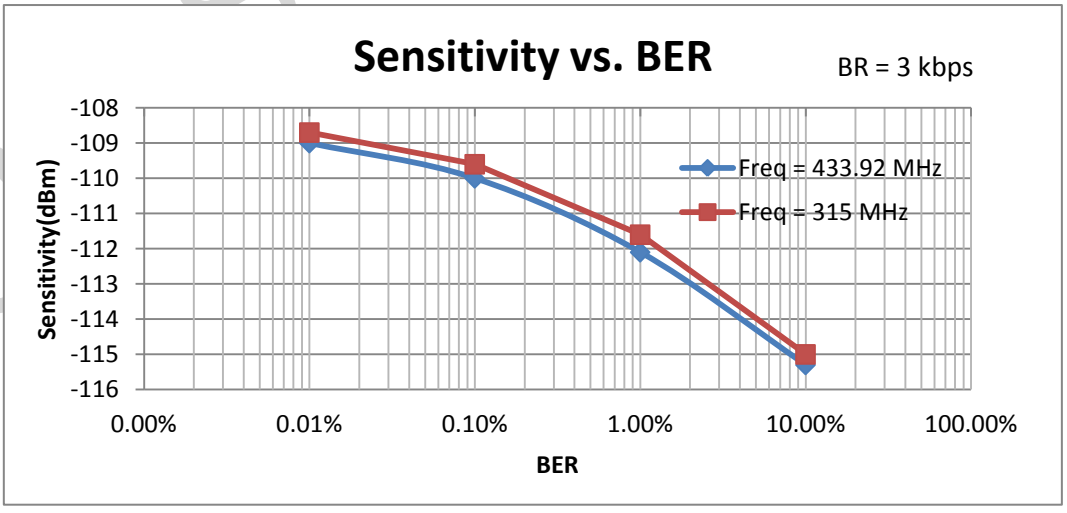


Figure 8. Sensitivity vs. BER

5 Function Description

As an integrated receiver with digital-analog hybrid design, the CMT2220LS chip applies LNA + Mixer + IF Filter + Limiter + PLL low-IF receiving architecture. It requires to connect 2 capacitors CAGC and CTH externally to assist in fulfilling the stability of the automatic gain control loop and the function of received data filtering.

5.1 Crystal Frequency and RF Frequency Point

The CMT2220LS applies a single-ended crystal oscillation circuit with the load capacitor required for crystal oscillation integrated in the chip. It is recommended to use a crystal with an accuracy of ± 20 ppm, an equivalent resistance of less than 60 Ω, and a load capacitance of 15 pF. Since crystal parasitic capacitance differs in different packaging specifications, users should pay more attention when selecting crystals to avoid receiver performance degradation caused by too much variance between the actual oscillation frequency and the target frequency value.

The CMT2220LS can operate in any frequency point within the free range 300 - 480 MHz. Users can fulfill different frequency points through selecting corresponding crystals. For instance, for a device operating at 433.92 MHz, the required crystal frequency is 13.52127 MHz. The formula between a specific RF operating frequency and the corresponding crystal frequency is as follows.

$$F_{XTAL} = \frac{13.52127}{433.92} F_{RF}$$

For example, for a CMT2220LS chip desired to operating at 315 MHz, the required crystal frequency is 9.81563 MHz.

5.2 Receiver IF Bandwidth

When the chip is operating at 433.92 MHz, the corresponding IF bandwidth is 510 kHz. The IF bandwidth is adjusted automatically with same proportion according to selected crystal frequency. The formula between a specific RF operating frequency and the corresponding IF bandwidth is as follows.

$$BW_{RF} = 1.175332e^{-3} * F_{RF}$$

For example the IF bandwidth is adjusted to 370 kHZ when the chip is operated at 315 MHz.

5.3 Considerations of CAGC and CTH Selection

The CAGC pin is the port for automatic gain control of receiving link, connecting with a filtering capacitor externally. The value of CAGC will affect the chip startup time, namely the larger the CAGC value, the longer the startup time. Suggest users choose a larger capacitor value in AC to DC applications while choose 1 uF or slightly smaller one in DC power supply applications.

Particularly, for CMT2220LS batches with the date code of line 2 marking assigned as *2009* or *2010*, users should make sure the #7 pin, with pin name NC, is connected to ground on PCB in applications. For the rest of CMT2220LS batches, the #7 pin functions no connection, it's ok to leave it floating in applications.

6 Ordering Information

Table 7. Ordering Information

Model	Description	Packaging	Packing Option	Operating Condition	Minimum Order Quantity
CMT2220LS-ESR[1]	300 - 480 MHz OOK receiver with 3.0 - 5.5 V supply power	SOP8	Tape and Reel	3.0 - 5.5 V, - 40 ~ 85 °C	2,500

Notes:

[1]. CMT2220LS refers to model CMT2220LS.

E refers to extended Industrial product rating, which supports temperature range from -40 to +85 °C.

S refers to the packaging type SOP8.

R refers to tape and reel packing type, and the minimum ordering quantity (MOQ) is 2,500 pieces.

Please visit www.cmostek.com for more product/product line information.
Please contact sales@cmostek.comor your local sales representative for sales or pricing requirements.

7 Packaging Information

The packaging information of CMT2220LS is shown in the below figure.

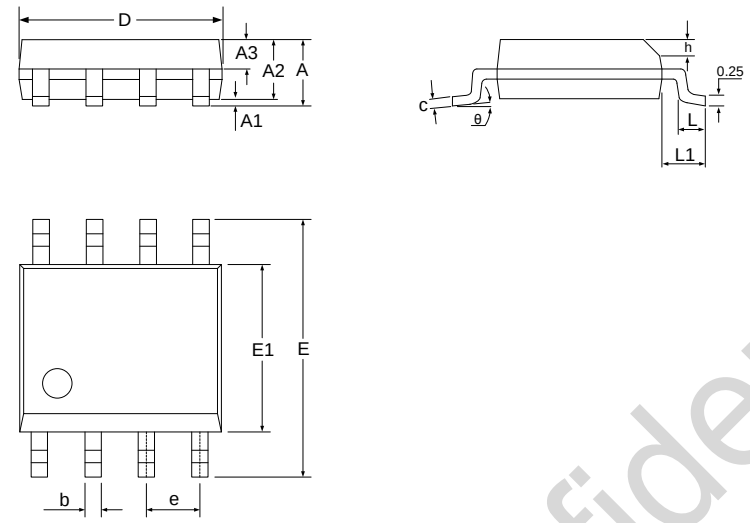


Figure 9. SOP8 Packaging

Table 8. SOP8 Packaging Scale

Symbol	Scale (mm)		
	Min.	Typ.	Max.
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.48
c	0.21	-	0.26
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05 BSC		
θ	0	-	8°

8 Top Marking

Figure 10. CMT2220LS Top Marking

Table 9. Top Marking Information

Marking Method	Laser
Pin 1 Mark	Diameter of the circle = 0.5 mm
Font Height	0.6 mm, align right
Font Width	0.3 mm
Line 1 Marking	CMT2220LS referring to model CMT2220LS
Line 2 Marking	YYWW is the date code assigned by the packaging factory. YY is the last 2 digits of the year. WW is the working week. ①②③④⑤⑥ is the internal tracing code.

9 Revise History

Table 10. Revise History Records

Version No.	Chapter	Description	Date
0.5	All	Initial version	2020-03-12
0.6	All	1. Change the pin 7 name of CMT2220LS from CTH to NC and change related function descriptions as follows. · For CMT2220LS, if the first 4 digits of the batch information in line 2 top mark is *2009* or *2010*, the pin 7 is required to be grounded or connected with a capacitor on the PCB when these chips are used. · For the rest of all CMT2220LS batches, the function of pin 7 is no connection , so that just leave it floating when these chips are used. · Add information for CAGC value affecting on chip startup time.	2020-04-15
0.7	3	Update R1 resistor description in Table 6 .	2020-05-14
0.8	All	Document refining.	2020-07-27

10 Contacts

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